LISTING OF THE CLAIMS

1. (currently amended) An nxm switch module for use in the first stage of an NxN multi-stage optical switching architecture, comprising:

sufficient input and output ports to satisfy the Clos nonblocking criteria;

at least one extra input port;

at least one extra output port;

where at least one of the extra ~~input and~~ output ports are ~~unallocated~~ used for fault isolation.

2. (currently amended) An nxm switch module for use in the final stage of an NxN multistage optical switching architecture, comprising:

sufficient input and output ports to satisfy the Clos nonblocking criteria;

at least one extra input port;

at least one extra output port;

where at least one of the extra ~~input and~~ output ports are ~~unallocated~~ are used for fault isolation.

3. (original) The switch module of claim 1, where further additional spare ports are added such that n=m.

4. (original) The switch module of claim 2, where further additional spare ports are added such that n=m.

5. (currently amended) A multi-stage optical switching architecture, comprising:

an input stage;

at least one middle stage;

and an output stage,

where the first stage comprises a plurality of the switch modules of either of claims 1 or 3~~; and~~

~~the second stage comprises a plurality of the switch modules of either of claims 2 or 4~~.

6. (original) The architecture of claim 5, where the middle stage comprises 2n-1 mxm switch modules which are allocated; and
one mxm switch module which is unallocated.

7. (original) The architecture of claim 6, further comprising a 1 x y switch or splitter, each of whose outputs are connected to a spare port in each of the first stage switch modules.

8. (original) The architecture of claim 6, where the input of the 1 x y switch or splitter is connected to an external light source.

9. (original) The architecture of either of claims 6-8, further comprising a y x 1 switch or selector, each of whose inputs are connected to a spare port in each of the final stage switch modules.

10. (previously withdrawn) A method of fault isolation for a nonblocking multistage optical switching architecture, comprising:
(a) obtaining the switch modules and ports thereof impacted in the fault;
(b) reconnecting the switching architecture at a given stage so as to bypass at least one of the input and output ports of the impacted switch module in that stage;
(c) keeping all other connections as originally configured;
(d) determining if the fault has abated; and

(e) repeating steps (b) through (d) at least once for each stage in the switching architecture.

11. (previously withdrawn) The method of claim 10, where the switching architecture is reconnected such that the input port of the impacted switch module is bypassed in the input stage.

12. (previously withdrawn) The method of claim 10, where the switching architecture is reconnected such that the output port of the impacted switch module is bypassed in the final stage.

13. (previously withdrawn) The method of claim 10, where the switching architecture is reconnected such that both the input and output ports of the impacted switch module are bypassed in each middle stage.

14. (previously withdrawn) The method of claim 10, where the switching architecture is reconnected such that in each stage, both the input and output ports of the impacted switch module are bypassed.

15. (previously withdrawn) The method of any of claims 10-14, where whether the fault has abated is determined by measuring the signal power through the reconnected path.

16. (previously withdrawn) The method of claim 15, where the signal power is measured via at least one of an external or an internal power monitor.

17. (previously withdrawn) The method of claims 10 or 11, where when the input port of the impacted first stage switch module is bypassed, at least one of an external signal

source or a dedicated fault isolation transmitter is utilized.

18. (previously withdrawn) The method of claim 17, where the external signal source is arranged such that its output power is equivalent to the nominal input power of the cross-connect.

19. (original) The architecture of claim 9, where the output of the y x 1 switch or selector is connected to at least one of an external power monitor or a dedicated fault isolation receiver.

20. (previously withdrawn) An article of manufacture comprising a computer-readable medium having stored thereon instructions adapted to be executed by a processor, the instructions which, when executed, cause the processor to manage fault isolation for a nonblocking multistage optical switching architecture, comprising:

(a) obtaining the switch modules and ports thereof impacted in the fault;

(d) reconnecting the switching architecture at a given stage so as to bypass at least one of the input and output ports of the impacted switch module in that stage;

(e) keeping all other connections as originally configured;

(d) determining if the fault has abated; and

(e) repeating (b) through (d) at least once for each stage in the switching architecture.

21. (previously withdrawn) The article of claim 20, where the article is integrated with the nonblocking multistage optical switching architecture.

22. (previously withdrawn) The article of claim 21, where the article is further integrated with a built in fault

isolation light source and power monitor.

23. (previously withdrawn) The article of claim 20, wherein the instructions when executed further cause the switching architecture to be reconnected such that the input port of the impacted switch module is bypassed in the input stage.

24. (previously withdrawn) The article of claim 23, wherein the instructions when executed further cause the switching architecture to be reconnected such that the output port of the impacted switch module is bypassed in the final stage.

25. (previously withdrawn) The article of claim 24, wherein when the instructions are executed further causes further cause the switching architecture to be reconnected such that both the input and output ports of the impacted switch module are bypassed in each middle stage.

26. (previously withdrawn) The article of claim 25, wherein when the instructions are executed further causes the switching architecture to be reconnected such that in each stage, both the input and output ports of the impacted switch module are bypassed.

27. (previously withdrawn) The article of any of claims 23-26 wherein when the instructions are executed further causes the determination of whether the fault has abated to be effected by measuring the signal power through the reconnected path.

28. (new) A multi-stage optical switching architecture, comprising:
an input stage;
at least one middle stage;

and an output stage,
where the first stage comprises a plurality of the switch modules of claims 1; and
the second stage comprises a plurality of the switch modules of either of claims 2 or 4.

29. (new) The architecture of claim 28, where the middle stage comprises 2n-1 mxm switch modules which are allocated; and one mxm switch module which is unallocated.

30. (new) The architecture of claim 29, further comprising a 1 x y switch or splitter, each of whose outputs are connected to a spare port in each of the first stage switch modules.

31. (new) The architecture of claim 29, where the input of the 1 x y switch or splitter is connected to an external light source.

32. (new) The architecture of either of claims 29-31, further comprising a y x 1 switch or selector, each of whose inputs are connected to a spare port in each of the final stage switch modules.